EXHIBIT A

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JUL 29 2004

OFFICIAL

Docket No.: 50432-067 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Kai Yang et al.	:	Confirmation Number:
Serial No.: 09/817,056	:	Group Art Unit: 2811
Filed: March 27, 2001	:	Examiner: T. Nguyen

For: STABILIZING FLUORINE ETCHING OF LOW-K MATERIALS

DECLARATION UNDER 37 C.F.R. §1.131

Mail Stop Declaration
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

We, Kai Yang, Darrell Erb and Fei Wang, hereby declare that:

1. We are the inventors of the invention disclosed and claimed in the above-referenced United States patent application.

2. We are aware of the prosecution history of this application which was filed in the U.S. Patent and Trademark Office on March 27, 2001. We are also aware that claims in the application have been rejected under 35 U.S.C. §102 for lack of novelty and under 35 U.S.C. §103 for obviousness predicated primarily upon U.S. Patent 6,521,533 issued to Morand et al. on February 18, 2003, based upon a PCT application filed on September 12, 2000.

Serial No.: 09/817,056

3. To our knowledge and in view of the factual evidence supplied herewith, the present invention was conceived in the United States prior to September 12, 2000 the filing date of the Morand et al. patent, as evidenced by the attached invention disclosure submitted to Advanced Micro Devices, Inc. (AMD), the assignee herein (Exhibit A hereto). Due diligence was exercised from prior to the September 12, 2000 filing date of the Morand et al. application to the filing date of the present application on March 27, 2001.

4. We further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful statement may jeopardize the validity of the application or any patent issuing thereon.

Date	Kai Yang
May 3, 2004 Date	Darrell M Erb Darrell Erb
Date	Fei Wang

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4/28/04	Kai Yang
Date	Kai Yang
Date	Darrell Erb
Date	Fei Wang

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Date	Kai Yang
Date	Darrell Erb
4-13-04 Date	Fei Wang

AMD INVENTION DISCLOSURE

TLD ID# [redacted] Rec'd date _____
Sunnyvale x42110, return to MS68. Texas x55964 return to MS562

F0424

Project: ☐, Product: ☐, Process: ☐, Technology ☑, to which the invention applies (*identify*):

List 2 to 5 key words useful to search by to find patents or art related to this invention:
Damascene Process Using Dielectric Barrier Films two different

Working title of invention: _____

INVENTOR/SESSION PARTICIPANT ADDRESS INFORMATION IS ON THE NEXT PAGE

Inventor's signature : Kai Yang date :_____
Inventor's printed full name: Kai Yang Citizenship:_____
Employee #:_____ Extension:_____ Mail stop:_____ Home telephone:( )_____
Division:_____ Directorate:_____ Dept #:_____ Dept :_____ Manager:_____
Residence address:_____
Post Office address:_____

Co-Inventor's signature : [redacted] Darrell Erb date :_____
Co-Inventor's printed full name: [redacted] Citizenship:_____
Employee #:_____ Extension:_____ Mail stop:_____ Home telephone:( )_____
Division:_____ Directorate:_____ Dept #:_____ Dept :_____ Manager:_____
Residence address:_____
Post Office address:_____

Co-Inventor's signature : _____ date :_____
Co-Inventor's printed full name:_____ Citizenship:_____
Employee #:_____ Extension:_____ Mail stop:_____ Home telephone:( )_____
Division:_____ Directorate:_____ Dept #:_____ Dept :_____ Manager:_____
Residence address:_____
Post Office address:_____

Co-Inventor's signature : Fei Wang date :_____
Co-Inventor's printed full name: Fei Wang Citizenship:_____
Employee #:_____ Extension:_____ Mail stop:_____ Home telephone:( )_____
Division:_____ Directorate:_____ Dept #:_____ Dept :_____ Manager:_____
Residence address:_____
Post Office address:_____

List on additional sheet if there are more co-inventors and list total number of inventors here:_____

Name(s) of attorney(s) preferred by inventor(s) to prepare patent application, if known:

LAW FIRM: MCDERMOTT, WILL & EMERY—John Hankins and Arthur Steiner

Witness 1 initial: _____ Witness 2 initial: _____

AMD INVENTION DISCLOSURE TLD ID# _____ Rec'd date _____
Sunnyvale x42110, return to MS68, Texas x55964 return to MS562

Identify known relevant art (patents, publications, products): _____

State the problem solved by this invention: Use dielectric Film instead of metal barrier. Solve Step Coverage problem, Reduce Contact resistan Enhance electromigration, Reduce capacitance.

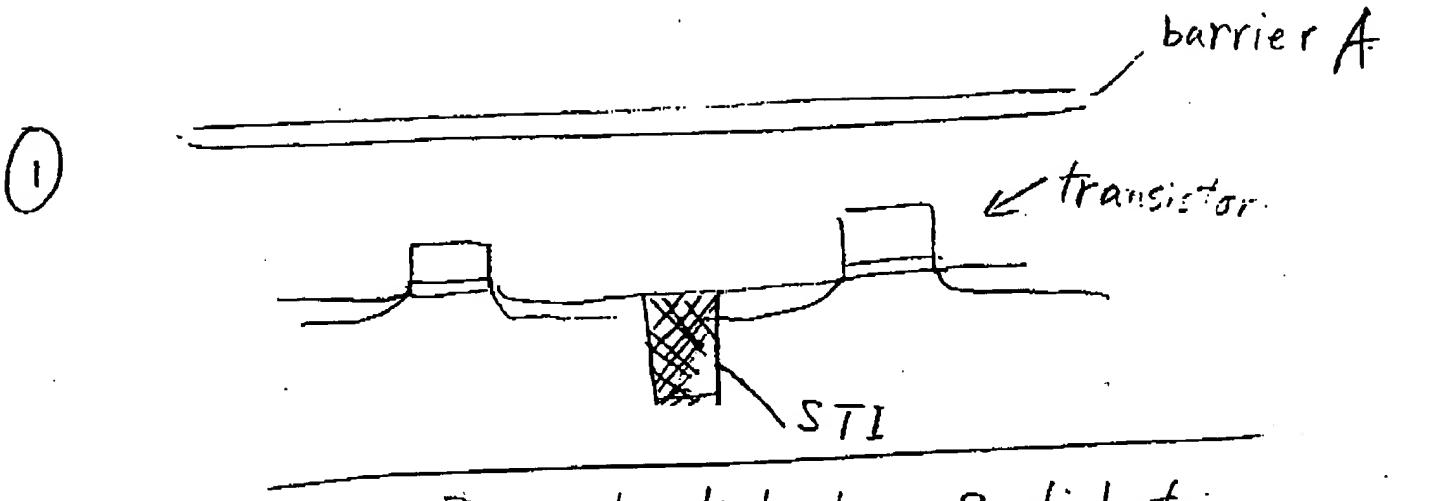
Brief description and/or sketch of invention (*please attach copies of AMD patent notebook pages, reports or drawings*): Current Copper Damascene technology use metal as barrier film such as Ta, TaN, Ti TiN WN, W etc. These films have much higher electrical resistivity than the Copper, ~~Ag~~ aluminum, or Silver. Some of these film can only be deposited using PVD at present (Sputtering), for example Ta, TaN, which have low conformal step coverage. Dielectric barrier film can be deposited by CVD process and hence have good step Coverage. These dielectric barrier film are SiN, SiC, etc. By using the process flow illustrated in the Figure, the barrier wall coverage can be more uniform. Because there is no metal barrier between the via and line, the contact resistance can be significantly reduced. The direct Copper via and Copper line Contact also enhance electromigration. Finally, at the Same metal line/via size, the parasitic capacitance is reduced.

Patent notebook # _____ Page numbers _____ Number of drawings _____

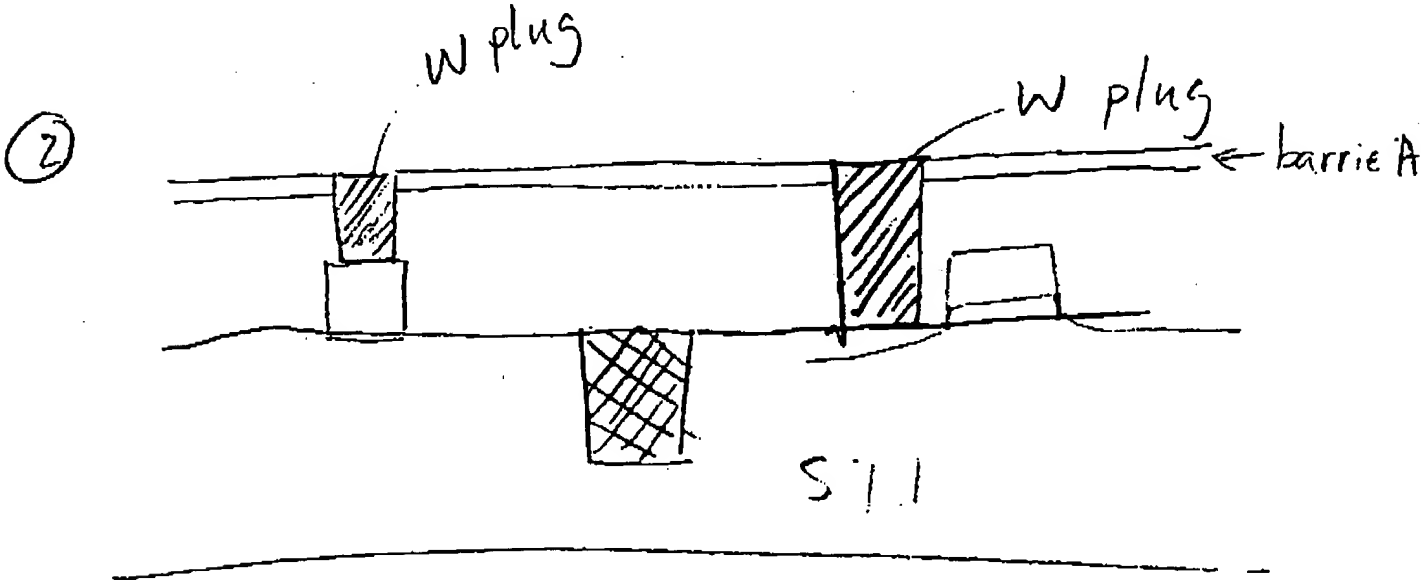
(2) Using Two different barrier film Solve possible misalignment problem.

Witness 1 initial: _____ Witness 2 initial: _____

Invention #67

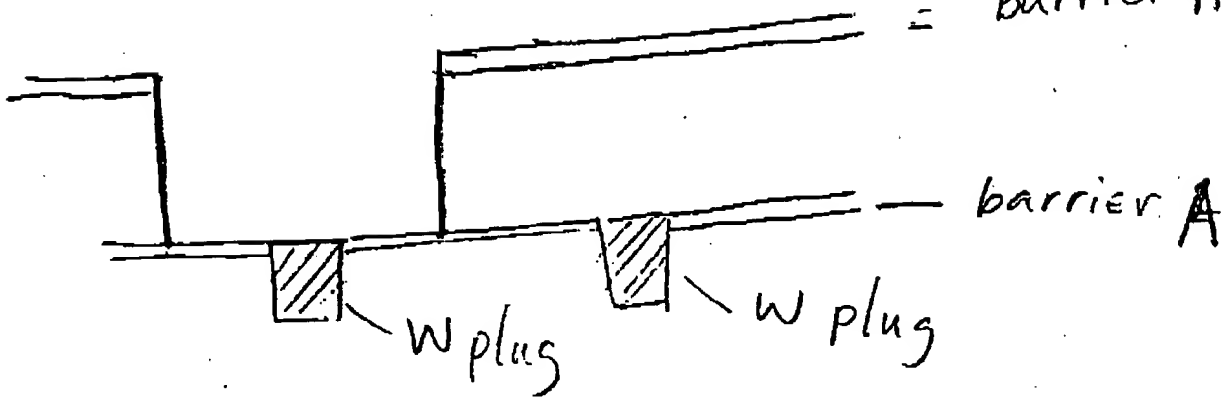


Deposit dielectric & dielectric barrierA after formation of Transistors



W plug formation

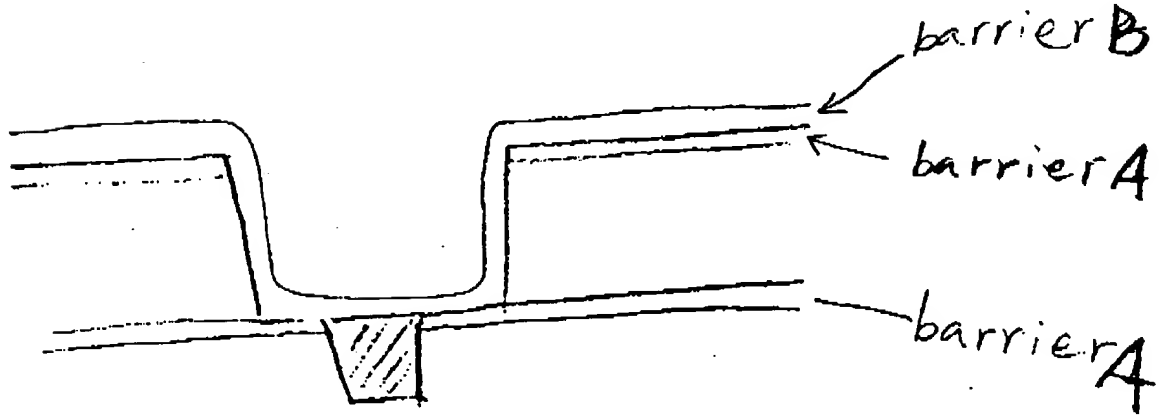
(3)



Deposition dielectric & barrier A

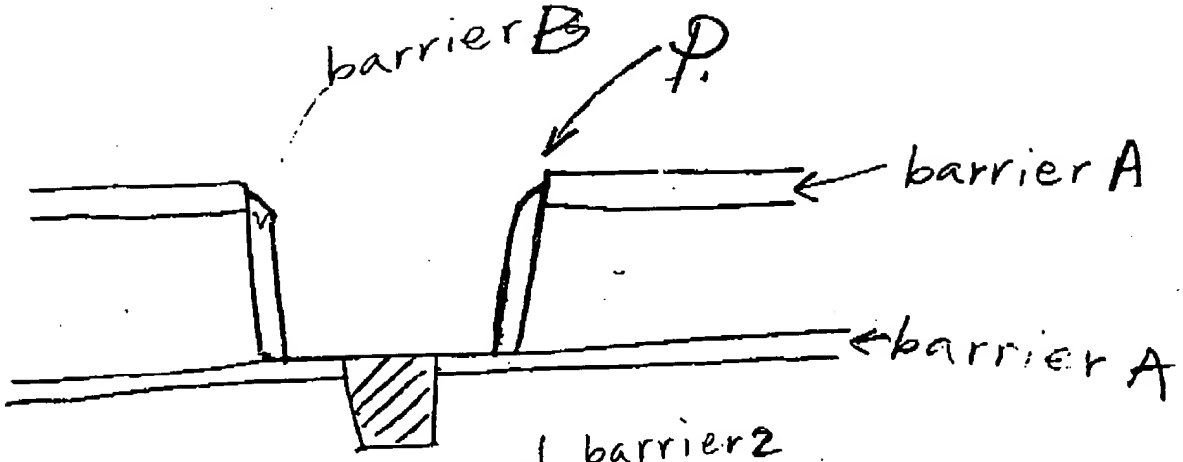
~~pattern~~ patterning, etch trench

(4)



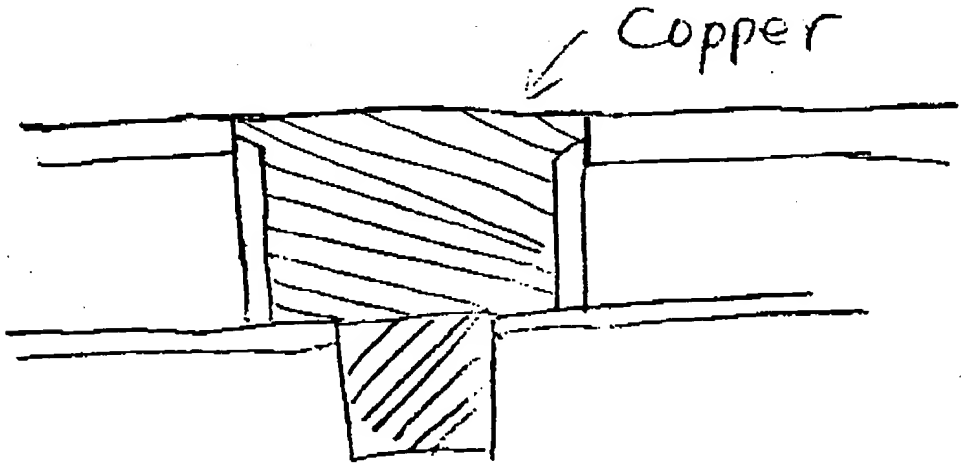
Deposition of barrier B film

(5)



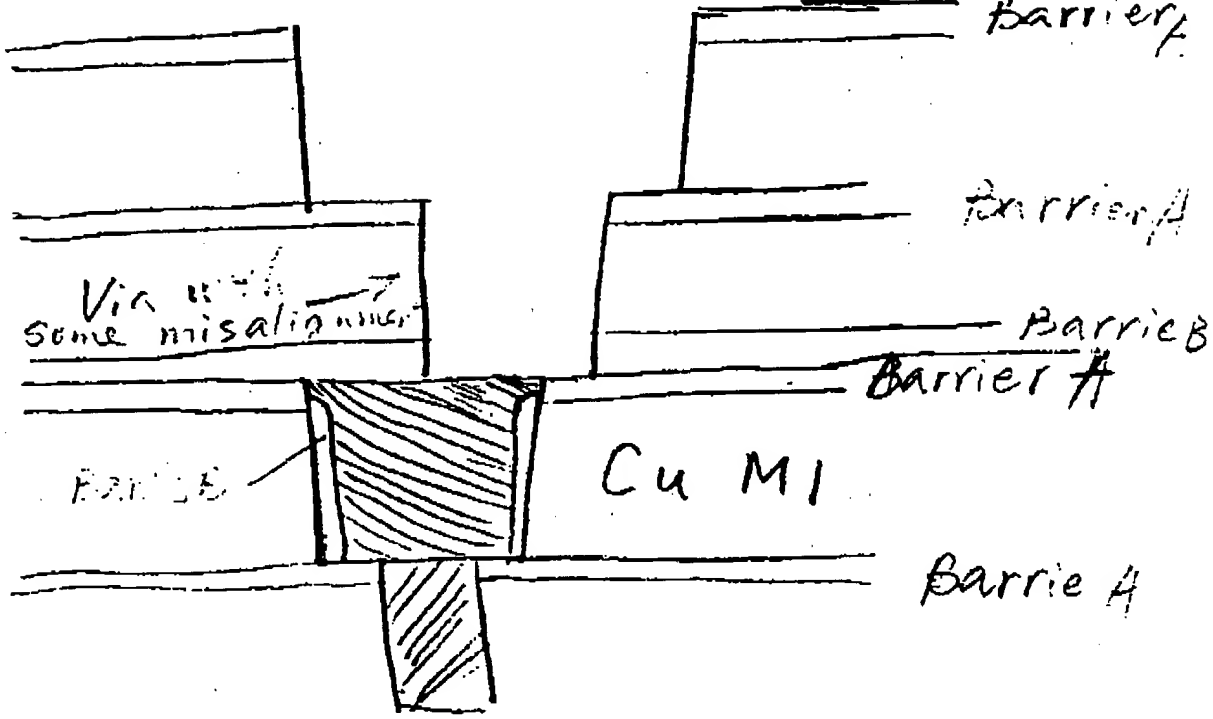
Unisotropic etch of barrier2 with selectivity to barrier A.
Barrier A thickness preferably thicker than that of barrier B, so that dielectric will not exposed at point P

(6)



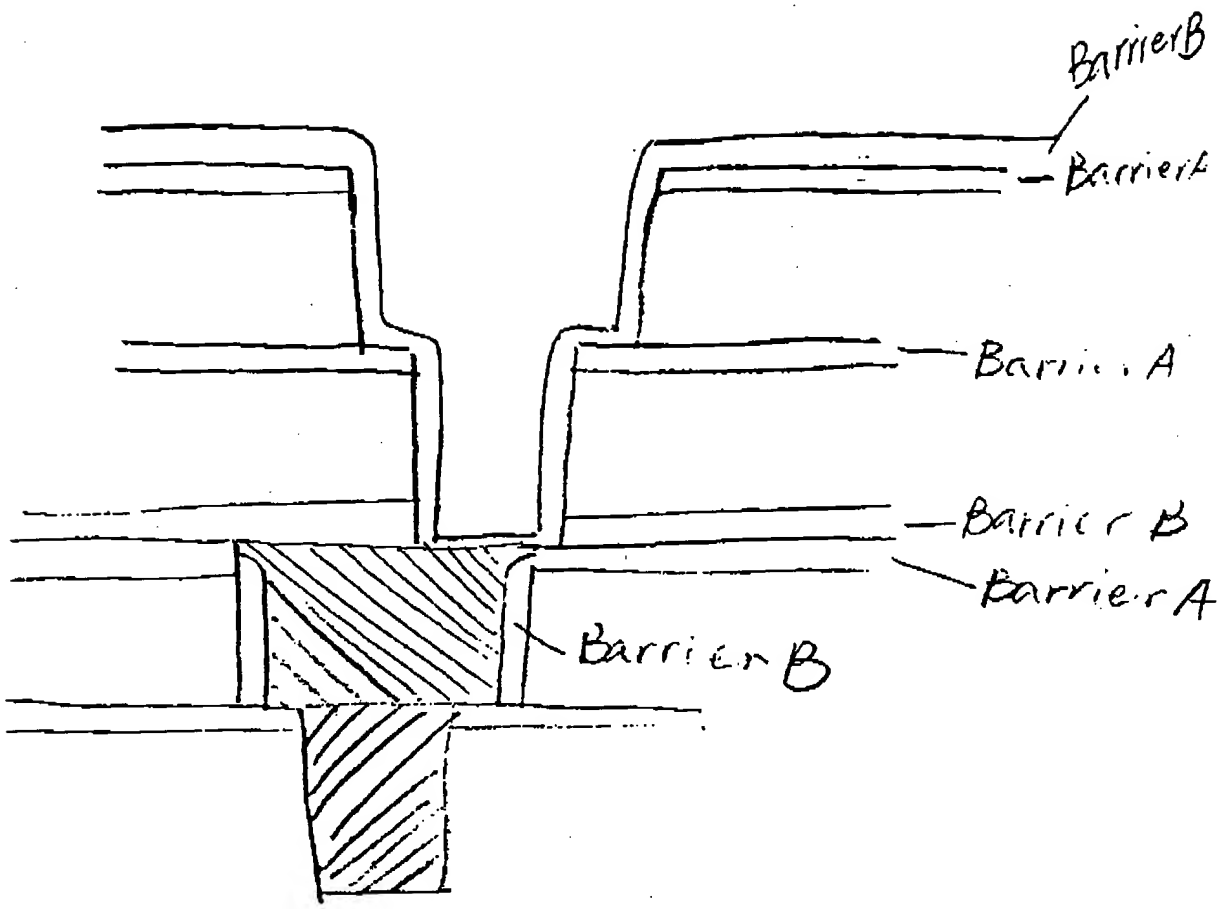
Fill Copper & CMP

Invention #67



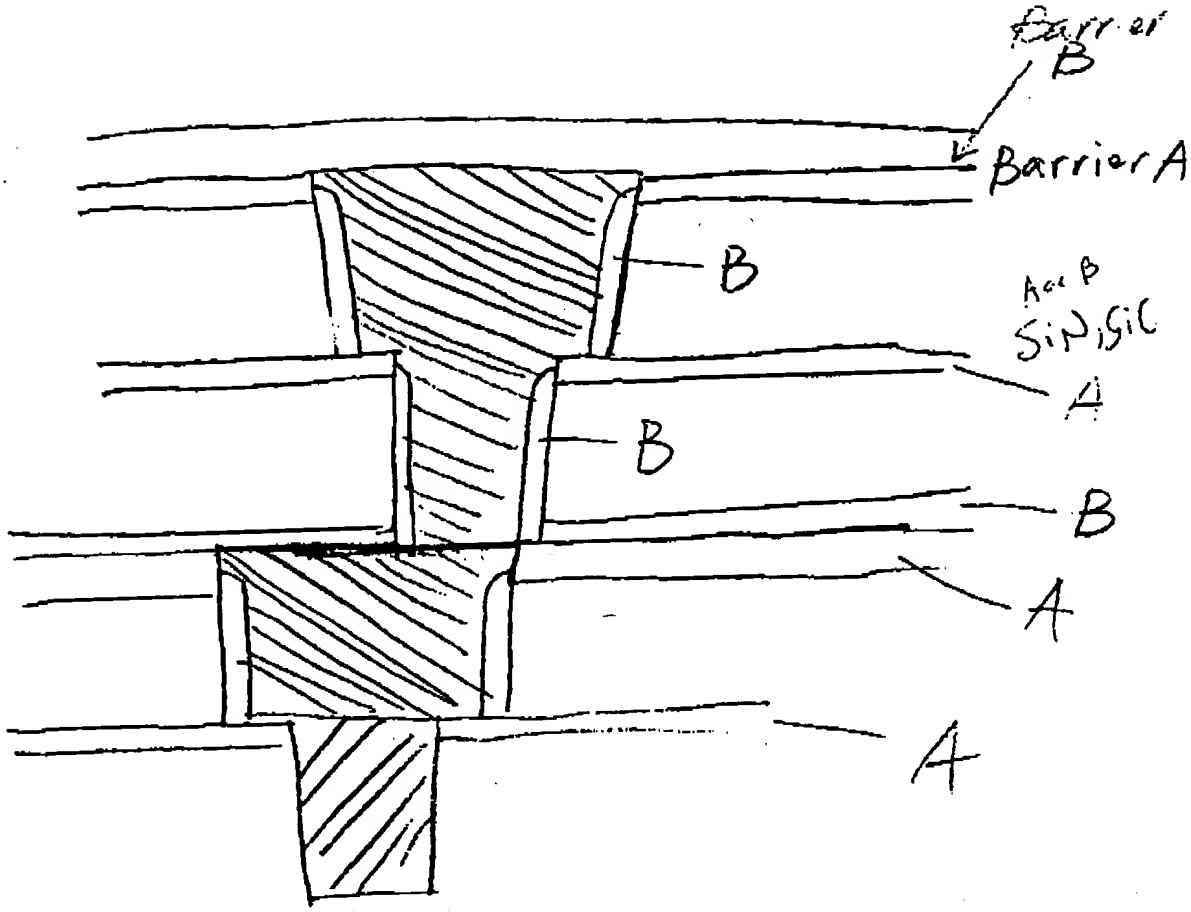
Deposition dielectric and barrier stack, patterning

8)



Deposit Barrier B.

(9)



Anisotropic etch barrier A

Fill with copper

Cap with barrier B